

The claim further recites that the system is responsive to a first request for allocation of memory space cacheable or non-cacheable type by "dynamically allocating" a block of memory from a page "free" status, the system thereafter changing the status of said page from "free" to "cacheable" or "non-cacheable" as the case may be and is responsive to a further request for allocation of memory space of cacheable or non-cacheable type, by "dynamically allocating" a block of memory from a page of appropriate status or, if such a block is unavailable, "dynamically allocating" a block from a page having "free" status, the system thereafter changing the status of said page from "free" to "cacheable" or "non-cacheable" as the case may be.

It is submitted that such features are neither disclosed nor implied by the prior art documents relied upon by the Examiner, either individually or in combination, as explained below.

U.S. Patent No. 4,885,680 (Anthony) teaches a system whereby memory is divided into areas intended for different uses, for example shared or local data. Shared memory areas are marked as non-cacheable and local memory areas are marked as cacheable, as in the present invention. However, in Anthony, the memory is divided up into such areas before any memory allocation takes place. This may be achieved by a program compiler or the system designer and results in the amount of memory available to any given class being fixed before execution of a program commences.

The technique disclosed in Anthony is described as "compile-time coherence" (column 7, line 24) which operates by "determining the cacheability of each datum during the creation of the program" (column 7, lines 33 to 35). Anthony further states that "the virtual address space is divided into classes corresponding to the cacheability classes. Then...data of a given class is allocated in an appropriate class of virtual memory.

Thus the address range may be interpreted to determine the cacheability class" (column 8, lines 14 to 20). Thus, it is submitted, Anthony clearly teaches that the address ranges (i.e. pages in the memory) for each type of memory are already established before any storage allocation is made.

This is clearly different to the system of the present invention where the allocation of cacheability class to the memory is wholly dynamic. The term "dynamically allocating" is a term of art and indicates the allocation of memory being determined at run-time. In other words, the cacheability status of both a block of data, and a page of memory, is determined during program execution rather than in a fixed way when the program is compiled.

In addition, as is clearly recited in new claim 13, the initial status of the system (i.e. before execution of the program) is that there is no division of memory to shared or local address ranges and all memory pages are marked as "free". A given memory page is only assigned a cacheability class in response to memory allocation requests during program execution.

When a first memory request for a particular class of memory is made, any "free" page may be used and is converted into a non-free page and marked "cacheable" or "non-cacheable" as appropriate. After the page is freed it may be used for data of a different storage class at a later time if program execution so determines and thus, during the lifetime of the system, a given memory page may be used for both shared and local allocations at different times.

This is entirely different concept from the invention disclosed in Anthony which therefore clearly draws the skilled person away from the invention defined in the claims of the present application. Moreover, the invention is extremely advantageous, particularly in systems where available memory is limited or where memory

A

usage patterns are hard to predict, since it allows maximum flexibility for the allocation of system memory.

USS,897,660 (Reinders) and USS,321,834 (Weiser) disclose the common practice of firstly allocating memory in separate pages and then sub-dividing the pages into blocks of the required size. The pages are marked as either "free" or "allocated". The Examiner suggests that the combination of either or Anthony/Reinders or Anthony/Weiser would result in a system having all of the featured recited in independent claim 14.

However, it is submitted that combining the allocation method of either Reinders or Weiser with the system of Anthony would result only in a system where memory pages are allocated from a predefined range of addresses according to the cacheability class. Since in Anthony the memory address ranges for local and shared memory are fixed during compilation of the program, one range of addresses (i.e. one set of pages) could only be allocated as either "cacheable" or "free". A memory page could therefore only be allocated if there is a free page already belonging to the right cacheability class.

It is respectfully submitted, therefore, that the skilled person would not be inclined to combine Anthony with either Reinders or Weiser in order to achieve the objects of the present invention. In any event, it is further submitted that any such combination would be lead to a system having all of the features recited in independent claim 14 of the present application. Amended claim 1 also recites the above-described features and it is therefore submitted that this claim is also novel and inventive over the prior art.

It is believed that the claims now pending are clearly allowable and notice to this effect is earnestly solicited.

It is respectfully submitted that this Amendment traverses and overcomes all of the Examiner's

A

originally filed. It is further submitted that this Amendment has antecedent basis in the application as originally filed, including the specification, claims and drawings, and that this Amendment does not add any new subject matter to the application. Reconsideration of the application as amended is requested. It is respectfully submitted that this Amendment places the application in suitable condition for allowance; notice of which is requested.

If the Examiner feels that prosecution of the present application can be expedited by way of an Examiner's amendment, the Examiner is invited to contact the Applicant's attorney at the telephone number listed below.

Respectfully submitted,

YOUNG & BASILE, P.C.

Darlene P. Condra

Darlene P. Condra
Attorney for Applicant(s)
Registration No. 37113
(248) 649-3333

3001 West Big Beaver Rd., Suite 624
Troy, Michigan 48084-3107

Dated: February 28, 2000
DPC/cmp

A